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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/978,442	10/16/2001	Christina M. Boyko	END 920000141US1	5327

7590

06/19/2002

Lawrence R. Fraley  
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EXAMINER

NORRIS, JEREMY C

ART UNIT

PAPER NUMBER

2827

DATE MAILED: 06/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/978,442

Applicant(s)

BOYKO ET AL.

Examiner

Jeremy Norris

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 17-20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9, 15 and 16 is/are rejected.
- 7) ☒ Claim(s) 10-14 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10/16/01 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

**DETAILED ACTION**

***Election/Restrictions***

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-16, drawn to a printed circuit board, classified in class 174, subclass 262.
- II. Claims 17-20, drawn to a method of making a printed circuit board, classified in class 29, subclass 852.

The inventions are distinct, each from the other because of the following reasons:

Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the circuit board of the invention of Group I could be formed by a subtractive process as opposed to the additive process claimed in the invention of Group II.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Mr. Lawrence Fraley (26,885) on 13 May 2002 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-16. Affirmation of this election must be made by applicant in replying

to this Office action. Claims 17-20 have been withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 4, 15 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 recites the limitation "said seal" in line 1. There is insufficient antecedent basis for this limitation in the claim. For examination purposes, Examiner assumes that this claim is to depend from claim 3 where a seal is recited.

Claim 15 recites the limitation "said first and second non-conductive layers" in line 2. There is insufficient antecedent basis for this limitation in the claim. For examination purposes, Examiner assumes that this refers to the first dielectric layer claimed in claim 6.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-9 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6,006,428, granted to Feilchenfeld et al. (hereafter Feilchenfeld).

Regarding claims 1-5, Feilchenfeld discloses, an interconnect structure comprising: a substrate (10) having first and second opposing surfaces and at least one internal side wall defining a through hole (26) within said substrate extending from said first opposing surface to said second opposing surface; a first conductive material (28) positioned on said at least one internal side wall of said substrate; a first conductive layer (25) positioned on a portion of said first surface of said substrate, said first conductive layer having a first layer portion (30) positioned over said through hole and electrically connected to said first conductive material on said internal side wall of said substrate; a second conductive layer (26) positioned on a portion of said second surface of said substrate, said second conductive layer having a first layer portion positioned over said through hole and electrically connected to said first conductive material on said internal side wall of said substrate; a first dielectric layer (34) positioned on said first conductive layer and said first opposing surface of said substrate and having at least one internal side wall defining an aperture in said first dielectric layer; and a second conductive material (38) positioned on said internal side wall of said first dielectric layer and including a portion of said second conductive material positioned on and electrically connected to said first layer portion of said first conductive layer [claim 1], wherein said first layer portion of said first conductive layer forms a seal over said first conductive material on said internal side wall of said substrate [claim 2], wherein said first layer portion of said second conductive layer forms a seal over said first conductive material on said internal side wall of said substrate [claim 3], wherein said seal comprises a metallurgical diffusion bond [claim 4], further including a chip

connector member (44) having a portion thereof positioned on said second conductive material [claim 5].

Regarding claims 6-9 and 15, Feilchenfeld discloses an interconnect structure comprising: a substrate (10) having first and second opposing surfaces and at least one internal side wall defining a through hole (26) within said substrate extending from said first opposing surface to said second opposing surface, wherein said substrate includes a metal layer (12) between said first and second opposing surfaces and first and second non-conductive layers (22 & 14, 16 & 24) positioned, respectively, between said first opposing surface and said metal layer and between said second opposing surface and said metal layer; a first conductive material (28) positioned on said at least one internal side wall of said substrate; a first conductive layer (25) positioned on a portion of said first surface of said substrate, said first conductive layer having a first layer portion (30) positioned over said through hole and electrically connected to said first conductive material on said internal side wall of said substrate; a second conductive layer (32) positioned on a portion of said second surface of said substrate, said second conductive layer having a first layer portion positioned over said through hole and electrically connected to said first conductive material on said internal side wall of said substrate; a first dielectric layer (34) positioned on said first conductive layer and said first opposing surface of said substrate and having at least one internal side wall defining an aperture in said first dielectric layer; and a second conductive material (38) positioned on said internal side wall of said first dielectric layer and including a portion of said second conductive material positioned on and electrically connected to said first layer portion of

said first conductive layer [claim 6], wherein said metal layer is selected from the group consisting of nickel, copper, molybdenum, iron, and alloys thereof (see col. 2, lines 40-55) [claim 7], wherein said metal layer comprises copper-Invar-copper [claim 8] further including a third conductive layer (18) positioned substantially within said first non-conductive layer [claim 9], wherein said first dielectric layer includes an effective modulus to assure sufficient compliancy of said interconnect structure during operation [claim 15].

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Feilchenfeld.

Feilchenfeld discloses the claimed invention as described above except Feilchenfeld does not specifically state that the effective modulus is from about 0.01 Mpsi to about 0.50 Mpsi. However, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to select the modulus to be in this range, since Feilchenfeld teaches that the dielectric is to be a "conformal coating" (see col. 2, line 20). The motivation for doing so would have been to match the needed properties of the device. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

#### ***Allowable Subject Matter***

Claims 10-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Claim 10 states the limitation "further including a fourth conductive layer within said first non-conductive layer and positioned between said third conductive layer and said metal layer". This limitation, in conjunction with the other claimed limitations was neither found to be disclosed in, nor suggested by the prior art.

#### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following documents disclose circuit board with stacked vias:

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US 4,665,468	Dohya,
US 4,729,061	Brown,
US 5,758,413	Chong et al.,
US 6,037,044	Giri et al..

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy Norris whose telephone number is 703-306-5737. The examiner can normally be reached on Mon.-Th., 9AM - 6:30 PM and alt. Fri. 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-7724 for regular communications and 703-305-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JCSN  
June 17, 2002



**KAMAND CUNEO**  
**PRIMARY EXAMINER**